A SCALABLE MMIC-COMPATIBLE POWER HBT

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ABSTRACT

A MMIC-compatible, scalable HBT, utilizing heatsinking through Au interconnects to local via-holes, is described. At 2.45 GHz, 960 μm^2 area HBTs exhibit 34.5 dBm output power, 15.5 dB gain and 57% PAE. At 10 GHz, 600 μm^2 HBTs have 33 dBm output, 8 dB gain, 47% PAE. Thermal impedance is reduced 40% on smaller devices, and the need for emitter ballasting is eliminated.

INTRODUCTION

Aluminum Gallium Arsenide/ Gallium Arsenide Heterostructure Bipolar Transistor (AlGaAs/GaAs HBT) have recently demonstrated exceptionally high output power density[1], and excellent power performance in hybrid amplifiers, both narrowband [2] and broadband.[3] An HBT that exploits the potentially high power density and is fully compatible with a standard monolithic microwave integrated circuit (MMIC) process is desired. To reach higher output power from a unit device requires the reduction of parasitic elements which limit the HBT performance as the emitter area is scaled up to large sizes. In addition, managing the heat generated during power operation is important in determining the ultimate size power device. Ballasting individual emitter elements in a distributed device is a technique used to avoid unequal current distribution but requires a penalty to be paid in the device gain. We have demonstrated an HBT device technology which addresses the scaling and thermal management issues and which is MMIC compatible.

An AlGaAs/GaAs HBT for MMIC power amplifiers is described. The layout of the transistor allows for scaling to large areas with excellent results. Localized through-wafer via holes are provided to each pair of unit cells, as illustrated in Figures 1 and 2. This eliminates the problem of increased inductance to ground as the HBT is scaled up by increasing the number of unit cells. The fabrication process for these HBTs is fully compatible with a standard MMIC process and does not require any additional novel heatsinking techniques, such as flip-chip mounting. Non-

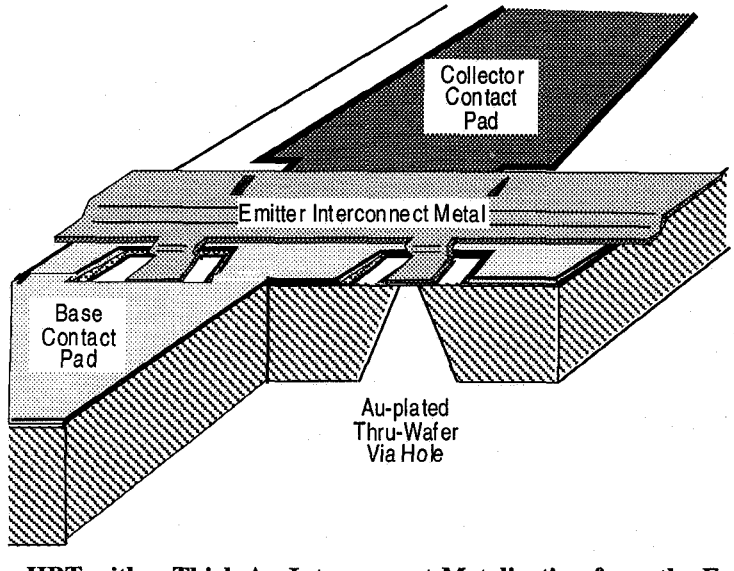

Fig. 1. An Illustration of the HBT with a Thick Au Interconnect Metalization from the Emitter Fingers to Local Through-Wafer Via Holes for Better Thermal Management and Lower Inductance.

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uniform current injection through the transistor due to localized heating, which causes current gain collapse, is avoided by using a thick Au metalization to provide a "thermal short" between emitter fingers.[1] By addressing the thermal issue directly, the requirement for ballasting, with the associated compromise in performance, is eliminated. The thick Au interconnects also lowers the HBT thermal impedance to improve the overall power handling capability of the device.

MATERIAL AND FABRICATION

The material structure from which these HBTs are fabricated is optimized for high gain performance at X-band and higher frequencies.[4] It includes a 5000Å thick collector layer and a 750Å base layer doped 5 x 10^{19} cm^{-3}. The devices are mesa-style microwave power transistors utilizing fully self-aligned emitter, base and collector ohmic contacts to minimize parasitics. The MMIC-compatible process includes two levels of Au interconnect metal which are used for formation of passive circuit elements (eg. capacitors, airbridges, transmission lines). A 3 μm thick Au layer, used for airbridges and transmission lines, serves as the connection between emitter fingers and via holes to the backside groundplane, see Figures 1 and 2. The vias are close to the active device minimizing parasitics and improving performance.[4]

MEASURED RESULTS

Common emitter measurements have been made on HBTs with emitter contact areas ranging from 240 μm^2 to 960 μm^2. Power data taken at 2.45 GHz and 10 GHz are presented. For measurement, HBTs were soldered onto carriers and bonded into power tuning jigs. These jigs consisted of transmission lines with "chicken dots" along the edges of the lines for tuning. Metal disks of varing size were moved along the transmission lines to tune the devices. A 10 GHz quarterwave transformer was also included on the jig to help match the input and output impedance. At 2.45 GHz, adjustable slug tuners were used in addition to the chicken dots to assist in tuning the devices. Jig losses (0.15 dB at 2.45 GHz, 0.4 dB at 10 GHz) were removed from all measurements to de-embed the data down to the device terminals.

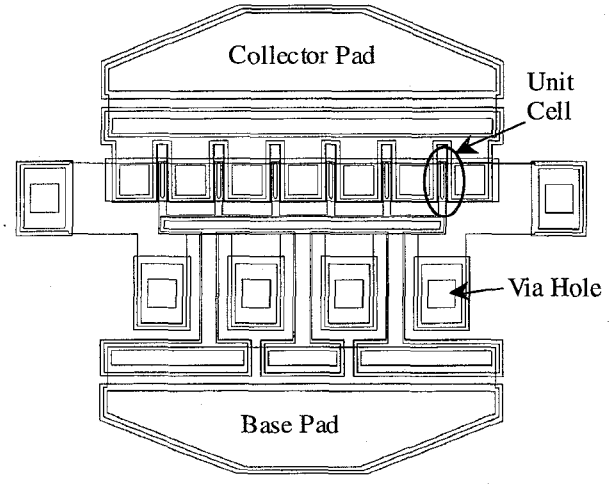

Fig. 2. The Layout Schematic of a 240 mm^2 Emitter Area HBT with Thick Au Interconnnects Between the Unit Cell Emitter Finger and the Local Via Holes. The emitter fingers are 2x20 mm^2.

Table 1. HBT Power Data at 2.45 and 10 GHz - Vce = 7 V

AREA (μm)	Pout (dBm)	Gp (dB)	PAE (%)
	2.45 GHz		
240	30.0	16.9	61.9
480	32.0	18.0	59.9
600	33.0	17.0	57.7
960	34.5	15.5	56.8
	10 GHz		
240	29.7	9.2	50.6
480	32.0	8.0	47.4
600	32.9	7.9	47.0

Excellent power performance is obtained at 2.45 GHz as shown in Table 1. The 960μm^2 area HBT, biased at 7 V, generates 34.5 dBm output power at 2 dB compression when tuned for power. The associated gain and power-added efficiency are 15.5 dB and 57% for this device. Smaller area HBTs exhibit higher gain and efficiency as described by Table 1. The 960 μm^2 emitter area HBT operates at a power density of 2.9 mW/μm^2. The 240 μm^2 HBT power density increases to 3.7 mW/μm^2 while maintaining excellent performance. The maximum output power, and the bias current, scale with area at approximately the same rate, shown in Figures 3 and 4. Ideally, output power should increase at a rate of 3 dBm per area doubling. The measured rate is 2.33 dBm/doubling.

The output power of the transistor is independent of frequency. A 600 μm^2 emitter area HBT generates 33 dBm at 2.45 GHz and at 10 GHz with 7 volt bias. The gain and efficiency are frequency dependent dropping from 17 dB and 58% at 2.45 GHz to 8 dB and 47% at 10 GHz. Data comparing the best power perfomance at 10 and 2.45 GHz for various size HBTs is presented in Table 1. Matching of input and output for the large emitter area HBTs is non-trivial due to the low impedances presented at the ports. Our best power results to date at 10 GHz are obtained on

the 600 μm^2 emitter area HBT because the test jigs available could not be used for larger devices. Despite this limitation, the resulting power and associated gain is among the best for 10 GHz operation. At 2.45 GHz, we were able to use existing jigs for tuning of larger area devices.

THERMAL CONSIDERATIONS

The thermal impedance, Rth, of the present layout HBT is significantly improved over Raytheon's older style device. The older style HBT does not have the thick Au metallization connecting the emitter fingers to the via holes. Instead, the metallization for the emitter ohmic contact serves as the interconnect between the active device and pads off the device mesa. This is a thin Au layer relative to the 3μm Au layer in the device described here. Thus the thermal dissipation in the older style device is only through the GaAs substrate. R_{th} is measured by changing the dc power dissipation in the HBT and monitoring the base-emitter voltage, Vbe. The change of Vbe provides a measure of temperature in the transistor.[5] The present layout reduces R_{th} by 40% over the older layout for identical unit cell dimensions fabricated on the same wafer. HBTs with two unit cells composed of a single 2x20 μm^2 emitter finger for a total of 80 μm^2 emitter area are compared. For the present layout HBT, R_{th} is 310 C/W. For comparison, R_{th} of Raytheon's older style HBT is 540 C/W. This reduction is due to the thick Au connecting the emitter finger over a short path to the through-wafer via holes. The vias are a low impedance path to the heatsink. The 310 C/W also compares well with the estimated value, 350 C/W, of the 60 μm^2 area HBT of [1]. For the present layout, heatsinking via the interconnects is very important in the thermal characteristics of the HBT and could be further improved by thickening the Au interconnect layer.

The thick Au interconnect metal also serves to reduce thermal variations in the HBT. This is observed by looking for the locus of points in the collector I-V characteristic where a collapse of current gain occurs.[6] For the present layout, the locus is moved to higher dissipated powers in the I-V plane compared to the older style device without the thick Au interconnection. A comparison of I-V characteristics for the two style layout HBTs, fabricated from the same wafer, is presented in Figure 5. Collapse of current gain is not observed on the present layout HBT.

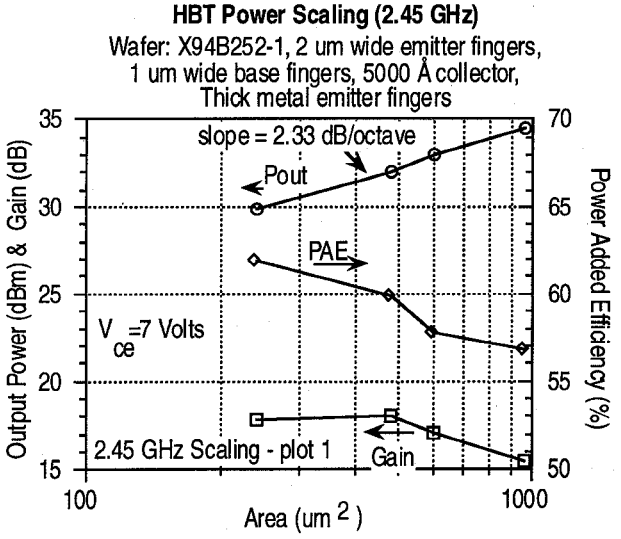

Fig. 3. HBT Power Scaling at 2.45 GHz with a Collector-to-Emitter Bias Voltage of 7V.

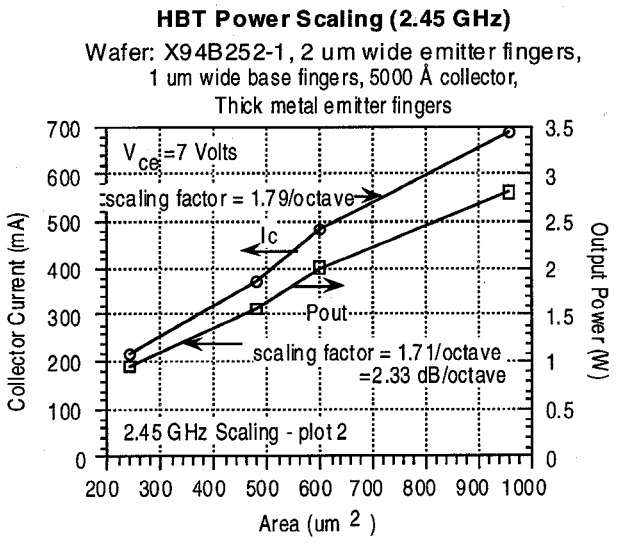

Fig. 4. HBT Current and Power Scaling of at 2.45 GHz for 7V Operation.

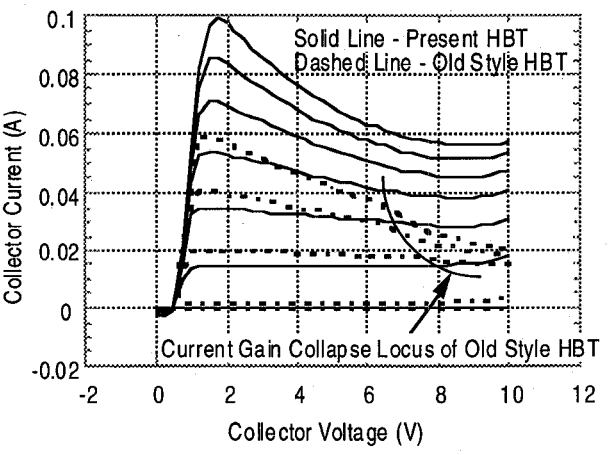

Fig. 5. Collector Current-Voltage Characteristics Demonstrate Improved Thermal Uniformity in the Present HBT by Elimination of Current Gain Collapse in Multi-cell HBTs.

CONCLUSION

The reported HBT layout achieves high power density and high total output power, by scaling to large emitter areas, with excellent gain and efficiency. This HBT design is fully compatible with standard MMIC processing, so the device is an excellent candidate for monolithic power amplifiers. The design exploits heatsinking through thick Au interconnects between the emitter fingers and localized via holes. This provides a low thermal impedance for the device, a reduction of 40% in R_{th} is achieved, and maintains excellent thermal uniformity in the device avoiding the onset of current gain collapse and eliminating the need for emitter ballasting.

ACKNOWLEDGMENT

The authors would like to express their appreciation and indebtedness to many colleagues at Raytheon. E. Tong, P. Saledas and J. Greathead for processing. V. Lacquio and B. Engel for assembly. M. Adlerstein, S. Shanfield, F. Schindler, and J. Callerame for support. A. Platzker, S. Bouthillette and C. Alfero for explaining previously encountered problems with large periphery PsHEMTs.

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